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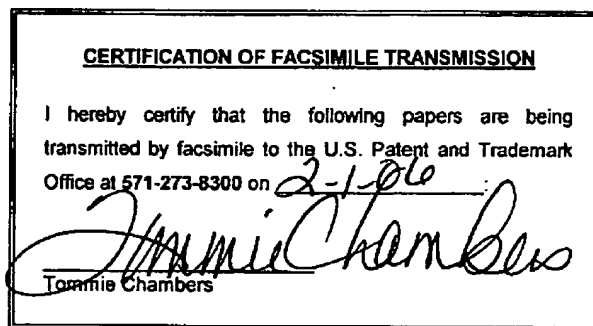
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mitchell Docket No: TI-35215AA
Serial No: 10/654,165 Examiner: Cunningham, Terry D.
Filed: 9/3/2003 Art Unit: 2816
For: APPARATUS AND METHOD FOR CONTROLLING OPERATION OF A
PROCESSOR DEVICE DURING STARTUP

APPEAL BRIEF PURSUANT TO 1.192(c)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:



The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final Office Action mailed June 7, 2005, and the Advisory Action mailed October 13, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

The only appeal that will directly affect or have a bearing on the Board's decision is serial number 10/640,981.

STATUS OF THE CLAIMS

Claims 1-20 were originally filed, and no claims have been cancelled or added.

Consequently, the subject matter of the instant appeal is the final rejection of Claims 1-20.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-20.

A Response After Final rejection was faxed to the Patent and Trademark Office on September 30, 2005, amending no claims.

The Advisory Action indicated that the Response had been considered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

FIG. 1 is a graphic representation of disadvantageous anomalies in a supply signal that may occur when a battery is inserted into a circuit. In FIG. 1, a graphic plot 10 illustrates a curve 12 representing a voltage signal measured according to volts indicated on a first axis 14 as a function of time indicated on a second axis 16. Curve 12 illustrates response of a voltage supply signal at power up of a battery powered device (not shown in FIG. 1). Curve 12 is at a minimal level during a time interval $t_0 - t_1$, during which time the battery (not shown in FIG.1) is not included in the battery powered device. Substantially at time t_1 , the battery is inserted into the device and curve 12 increases sharply. During a time interval $t_1 - t_2$, curve 12 experiences significant variance, indicating significant ringing, "glitching" or other disadvantageous anomalies or noise in the supply signal represented by curve 12. During times following time t_2 , curve 12 is substantially level at a constant voltage value, indicating that supply voltage has settled to a stable value.

FIG. 2 is an electrical schematic diagram illustrating the preferred embodiment of the apparatus of the present invention. In FIG. 2, an apparatus 20 for controlling operation of a processor 22 during startup includes a signal treating circuit 24 and an output circuit 26.

Signal treating circuit 24 includes a time-delay circuit 30 and a non-delay circuit 40. Time delay circuit 30 includes a resistor 32 and a capacitor 34 coupled in series between a voltage supply locus 28 and ground 29. A battery 25 is coupled between voltage supply locus 28 and ground 29 to provide a voltage supply signal V_{CC} to apparatus 20. Resistor 32 and capacitor 34 impose an RC (resistor-capacitor) time constant delay on signals traversing time delay circuit 30. A resistor 36 coupled in series with a reverse-biased diode 38 between capacitor 34 and voltage supply locus 28 provides a fast discharge path for capacitor 34. The fast discharge path through diode 38 and resistor 36 permits apparatus 20 to react quickly to negative excursions or "glitches" in voltage supply signal V_{CC} during operation when it may be necessary to reset processor device 22. Non-delay circuit 40 includes resistors 42, 44 coupled in series between voltage supply locus 28 and ground 29.

The fast discharge path through diode 38 and resistor 36 provide a significant operational advantage for the apparatus of the present invention as compared with prior art supply voltage supervisor (SVS) circuits. Many prior art SVS circuits impose a time delay (often preset and invariable) after voltage supply signal V_{CC} crosses a predetermined threshold before releasing the controlled processor from a reset condition. In contrast, by providing a fast discharge path for capacitor 34, apparatus 20 will hold processor device 22 as long as voltage supply signal V_{CC} is swinging or varying. Even if voltage supply signal V_{CC} is unstable (i.e., swinging or varying) for ten seconds, apparatus 20 would hold processor device 22 in reset for the entire ten seconds, plus an additional settling time.

Output circuit 26 includes a comparator 50. Comparator 50 receives a positive supply voltage V_+ at a positive supply locus 51 and receives a negative supply voltage V_- at a negative supply locus 53. Comparator 50 receives input signals at a non-inverting input locus 52 (input signal V_{IN+}) and at an inverting input locus 54 (input

signal V_{IN-}). Comparator 50 presents an output signal (output signal V_{OUT}) at an output locus 56. Comparator 50 receives time-delayed signal V_{IN+} at non-inverting input locus 52 from a juncture 35 between resistor 32 and capacitor 34 in time delay circuit 30. Comparator 50 receives non-delayed signal V_{IN-} at inverting input locus 54 from a juncture 43 between resistors 42, 44 in non-delay circuit 40. The voltage divider effect of resistors 42, 44 ensures that input signal V_{IN-} arriving at inverting input locus 54 is less than supply voltage V_{CC} . The time-delay effect of the RC circuit established by resistor 32 and capacitor 34 ensures that the level of input signal V_{IN+} appearing at non-inverting input locus 52 will rise relatively gradually over time as compared to the rate of increase of input signal V_{IN-} appearing at inverting input locus 54. Additionally, the fast discharge path provided by diode 38 and resistor 36 ensures that a rise in the level of input signal V_{IN+} is arrested or reversed when supply voltage signal V_{CC} deviates negatively. Thus, when power is initially supplied to apparatus 20 (e.g., as by inserting a battery or by closing a switch) output signal V_{OUT} presented by comparator 50 at output locus 56 is low because the potential of input signal V_{IN+} at non-inverting input locus 52 is less than the potential of input signal V_{IN-} at inverting locus 54. Output locus 56 is coupled with a reset pin or reset control pin 23 of processor 22. A low output signal V_{OUT} presented by comparator 50 at output locus 56 (as is the case when power is first provided to apparatus 20) applies a low signal to reset control pin 23 and holds processor 22 in a reset condition.

Delay imposed by time-delay circuit 30 and the amount of voltage dividing effected by non-delay circuit 40 may be adjusted to ensure that only after voltage supply signal V_{CC} has stabilized does non-inverting input locus 52 experience a higher potential than is present at inverting input locus 54 so that comparator 50 will present a high output signal V_{OUT} at output locus 56. Presence of a high output signal V_{OUT} at output locus 56 applies a high signal to reset pin 23, thereby releasing processor 22 for operation. Stabilization time experienced by apparatus 20 (i.e., the time period for which apparatus 20 can hold processor 22 in a reset state) is principally adjusted by selection of values for resistor 32 and capacitor 34, thereby adjusting the RC time constant of time-delay circuit 30. Values of resistors 42, 44 are preferably high to reduce current consumption by apparatus 20. In contrast, use of lower values for

resistor 32 carries no penalty because no current flows through the resistor 32 after voltage supply signal V_{CC} has stabilized.

The description of the structure and operation of apparatus 20 has been an exemplary explanation based upon a presumption that processor device 22 requires a low signal at reset pin 23 to keep processor device 22 in a reset condition. The teachings of the present invention can as easily be applied to advantage by one skilled in the art for creating a supply voltage supervisor (SVS) circuit for controlling a processor device (not shown in FIG. 2) that requires a positive signal at its reset pin to keep the processor device in a reset condition.

If resistor 32 has a value of $R1$, resistor 42 has a value of $R2$, resistor 44 has a value of $R3$, resistor 36 has a value of $R4$ and capacitor 34 has a value of C , one may design apparatus 20 to hold processor 22 in a reset state (i.e., with output signal V_{OUT} low) for a particular time interval (stabilization time of apparatus 20). By selection of $R1$, C , $R2$ and $R3$, a user can guarantee a reliable reset signal to processor 22 for a given dv/dt for voltage supply signal V_{CC} .

Voltages at comparator input loci 52, 54 are expressed:

$$V_{IN+} = V_{cc} - V_{cc} \times e^{-t/R1C} \quad [1]$$

and

$$V_{IN-} = V_{cc} \times \frac{R3}{R2 + R3} \quad [2]$$

In order to hold processor 22 in reset, one needs $V_{IN-} > V_{IN+}$. That yields:

$$V_{cc} \times \frac{R3}{R2 + R3} > V_{cc} - V_{cc} \times e^{-t/R1C} \quad [3]$$

Solving expression [3] for t:

$$t < -R1C \times \ln\left(\frac{R2}{R2 + R3}\right) \quad [4]$$

From expression [4], one can calculate the amount of time processor 22 will stay in reset. Therefore, as long as voltage supply signal V_{CC} ramps to a steady state in a faster time than the limit one can keep processor 22 in reset, one can be guaranteed of a reliable reset.

Reverse-biased diode 38 and resistor 36 provide a fast discharge path for capacitor 34. This fast discharge permits apparatus 20 to react quickly to negative excursions or glitches in voltage supply signal V_{CC} during normal operation which may make it desirable to reset processor 22. Resistor 36 allows a user to tune the response time of apparatus 20 for any supply voltage glitches that are expected. Removal of resistor 36 permits the fastest response time by apparatus 20 to variations in voltage supply signal V_{CC} , but may result in undesired resets for processor 22.

The current consumption of apparatus 20 is about 1 μ A (1 microampere; current consumption of comparator 50) plus the current through resistors 42, 44. Generally, the current consumption by apparatus 20 can be kept low, making apparatus 20 practical for use with battery-operated systems. Apparatus 20 costs less to manufacture than many dedicated SVS (supply voltage supervisor) systems.

FIG. 3 is a graphic representation of a variety of signals within the apparatus illustrated in FIG. 2 during start up. In FIG. 3, a graphic plot 70 illustrates a curve 72

representing voltage supply signal V_{CC} , a curve 74 representing input signal V_{IN+} (FIG. 2), a curve 76 representing input signal V_{IN-} (FIG. 2) and a curve 78 representing output signal V_{OUT} (FIG. 2). Curves 72, 74, 76, 78 are measured according to volts indicated on a first axis 80 as a function of time indicated on a second axis 82.

Curve 72 illustrates response of a voltage supply signal V_{CC} at power up of apparatus 20 (FIG. 2). Curve 72 is at a minimal level during a time interval $t_0 - t_1$, during which time battery 25 is not included in apparatus 20. Substantially at time t_1 , battery 25 is inserted into apparatus 20 and curve 72 increases sharply. During a time interval $t_1 - t_2$, curve 72 experiences significant variance, indicating significant ringing, "glitching" or other disadvantageous anomalies or noise in voltage supply signal V_{CC} represented by curve 72. During times following time t_2 , curve 72 is substantially level at a constant voltage value, indicating that voltage supply signal V_{CC} has settled to a stable value.

Curve 74 illustrates response of input signal V_{IN+} presented at non-inverting input locus 52 (FIG. 2). Curve 74 is at a minimal level during a time interval $t_0 - t_1$, during which time battery 25 is not included in apparatus 20. Substantially at time t_1 , battery 25 is inserted into apparatus 20 and curve 74 begins to rise or increase. The rate of increase of curve 74 during time interval $t_1 - t_3$ is less than the substantially immediate increase of curve 72 at time t_1 . The lesser rise rate of curve 74 vis-à-vis curve 73 reflects the influence of the RC time constant imposed by time delay circuit 30 (FIG. 2) on input signal V_{IN+} .

Curve 76 illustrates response of input signal V_{IN-} presented at inverting input locus 54 (FIG. 2). Curve 76 is at a minimal level during a time interval $t_0 - t_1$, during which time battery 25 is not included in apparatus 20. Substantially at time t_1 , battery 25 is inserted into apparatus 20 and curve 76 (representing input voltage signal V_{IN-}) increases sharply in a manner very similar to the behavior of curve 72 (representing voltage supply signal V_{CC}). This similarity of behavior of curve 76 as compared with curve 72 results from input signal V_{IN-} being presented from non-delay circuit 40 (FIG. 2) so that no time delay is imposed upon input signal V_{IN-} . The voltage divider action performed by resistors 42, 44 (FIG. 2) ensures that input signal V_{IN-} will have a lesser magnitude than is exhibited by voltage supply signal V_{CC} . During a time interval $t_1 - t_2$,

curve 76 experiences significant variance, indicating significant ringing, "glitching" or other disadvantageous anomalies or noise in input signal V_{IN-} similar to noise present in voltage supply signal V_{CC} represented by curve 72. During times following time t_2 , curve 76 is substantially level at a constant voltage value, indicating that input signal V_{IN-} has settled to a stable value.

Curve 78 illustrates response of output signal V_{OUT} presented at output locus 56 (FIG. 2). Curve 78 is at a minimal level during a time interval $t_0 - t_3$ because input signal V_{IN+} is not greater than input signal V_{IN-} during time interval $t_0 - t_3$. During time interval $t_0 - t_3$ when output signal V_{OUT} is low, reset pin 23 of processor device 22 (FIG. 2) is kept low so that processor device 22 is kept in a reset orientation and excursions of voltage supply signal V_{CC} do not affect operation of processor device 22. Substantially at time t_3 , input signal V_{IN+} exceeds input signal V_{IN-} for the first time. As a consequence, comparator 50 (FIG. 2) generates a high value for output signal V_{OUT} (curve 78), reset pin 23 is set at a high value and processor device 22 is released from its reset orientation and is free to operate. Apparatus 20 holds processor device 22 in a reset orientation until voltage supply signal V_{CC} is stabilized. Control of processor 22 by apparatus 20 is not dependent on any predefined supply voltage level or threshold, as is the case with prior art supply voltage supervisor (SVS) apparatuses. Rather, apparatus 20 controls operation of processor device 22 based upon stabilization time of voltage supply signal V_{CC} .

FIG. 4 is a flow diagram illustrating the preferred embodiment of the method of the present invention. In FIG. 4, a method 100 for controlling operation of a processor device during startup begins at a START locus 102. Method 100 continues with the step of, in no particular order: (1) providing a signal treating circuit, as indicated by a block 104; and (2) providing an output circuit coupled with the signal treating circuit, as indicated by a block 106. Method 100 continues with the step of operating the signal treating circuit to receive a voltage supply signal at at least one voltage supply locus, as indicated by a block 108. Method 100 continues with the step of operating the signal treating circuit to use the voltage supply signal for generating a first treated signal and a second treated signal, as indicated by a block 110.

Method 100 continues with the step of operating the output circuit to receive the first treated signal and the second treated signal, as indicated by a block 112. Method 100 continues with the step of operating the output circuit to generate a control signal at an output locus; the control signal being based upon a relationship between the first treated signal and the second treated signal, as indicated by a block 114. Method 100 continues with the step of providing the control signal to the processor device for effecting the controlling, as indicated by a block 116. Method 100 terminates at an END locus 118.

GROUND OF REJECTION

The two grounds of rejection are whether Claims 1-20 are unpatentable under 35 U.S.C. § 112, second paragraph; and secondly whether Claims 1-20 are unpatentable 35 U.S.C. § 102 as being anticipated by Nagano.

ARGUMENTS

The Examiner alleges that it is misdescriptive that the output signal controls the processor "only" during startup.

Claim 1 recites that the processor is controlled during startup by the output signal.

The word "only" does not appear in Claim 1.

Claim 1 is not misdescriptive.

Claims 1-20 are in full compliance with 35 U.S.C. § 112, and particularly pointing out and distinctly claiming the subject matter which they believe is their invention.

It is respectfully submitted that Nagano does not disclose or suggest the presently claimed invention including the processor being controlled during startup by the output signal in independent Claim 1, the processor being controlled during startup by the control signal in independent Claim 9, albeit defined as the step of controlling the processor during startup by the control signal in independent Claim 17.

The Examiner alleges that the processor device is intended use.

A rejection based on intent use is only valid when the phrase appears only in the preamble.


Here, the processor is in the body of the claim language and the intended use rejection is not properly applied.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-20 under 35 U.S.C. § 112 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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APPENDIX

Claim 1 (previously amended): An apparatus for effecting a controlled startup of a processor device; the apparatus comprising:

(a) a first signal-treating circuit coupled with a voltage supply locus; said first signal-treating circuit receiving a voltage supply signal and producing a first treated signal representing said voltage supply signal;

(b) a second signal-treating circuit coupled with said voltage supply locus; said second signal-treating circuit receiving said voltage supply signal and producing a second treated signal representing said voltage supply signal; and

(c) a comparing unit; said comparing unit having a first input locus coupled with said first signal-treating circuit and receiving said first treated signal; said comparing unit having a second input locus coupled with said second signal-treating circuit and receiving said second treated signal; said comparing unit generating an output signal at an output locus when said first treated signal has a predetermined relationship with said second treated signal; said output locus being coupled with said processor device; said processor device being controlled during startup by said output signal.

Claim 2 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

Claim 3 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 4(original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 2 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 5 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said comparing unit is a comparator.

Claim 6 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 5 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

Claim 7 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 5 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 8 (original): An apparatus for effecting a controlled startup of a processor device as recited in Claim 6 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 9 (previously presented): An apparatus for controlling operation of a processor device during startup of said processor device; the apparatus comprising:

(a) a signal treating circuit receiving a voltage supply signal at a voltage supply locus; said signal treating circuit using said voltage supply signal for generating a first treated signal and a second treated signal; and

(b) an output circuit coupled with said signal treating circuit; said output circuit receiving said first treated signal and said second treated signal and generating a control signal at an output locus based upon a relationship between said first treated signal and said second treated signal; said output locus being coupled with said processor device; said control signal effecting said controlling; said processor device being controlled during startup by said control signal.

Claim 10 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

Claim 11 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 12 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 10 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 13 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said output circuit comprises a comparator.

Claim 14 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 13 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

Claim 15 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 13 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 16 (original): An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 14 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

Claim 17 (previously presented): A method for controlling operation of a processor device during startup of said processor device; the method comprising the steps of:

(a) in no particular order:

(1) providing a signal treating circuit; and

(2) providing an output circuit coupled with said signal treating circuit;

(b) operating said signal treating circuit to receive a voltage supply signal at at least one voltage supply locus;

(c) operating said signal treating circuit to use said voltage supply signal for generating a first treated signal and a second treated signal;

(d) operating said output circuit to receive said first treated signal and said second treated signal;

(e) operating said output circuit to generate a control signal at an output locus; said control signal being based upon a relationship between said first treated signal and said second treated signal; and

(f) providing said control signal to said processor device for effecting said controlling; controlling said processor device during startup by said control signal.

Claim 18 (original): A method for controlling operation of a processor device during startup of said processor device as recited in Claim 17 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

Claim 19 (original): A method for controlling operation of a processor device during startup of said processor device as recited in Claim 18 wherein said output circuit comprises a comparator.

Claim 20 (original): A method for controlling operation of a processor device during startup of said processor device as recited in Claim 19 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.